

Automotive-grade N-channel 60 V, 27 mΩ typ., 20 A STripFET™ II Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

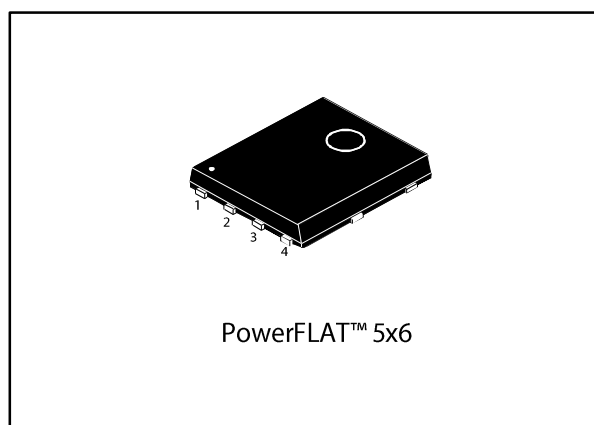
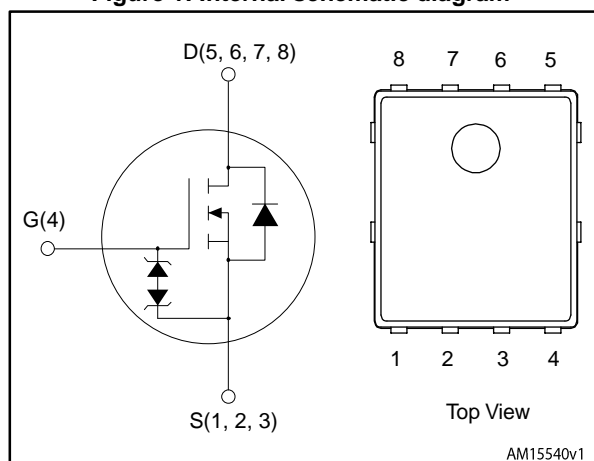


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STL20NF06LAG	60 V	40 mΩ	20 A	75 W

- Designed for Automotive applications and AEC-Q101 qualified
- PowerFLAT™ 5x6 with wettable flanks
- Logic level V_{GS(th)}
- Maximum junction temperature: T_J = 175 °C

Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STL20NF06LAG	20NF06L	PowerFLAT™ 5x6	Tape and reel

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package information	9
	4.1 PowerFLAT™ 5x6 WF type R package information	9
	4.2 PowerFLAT™ 5x6 WF packing information	11
5	Revision history	13

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)(2)}$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	20	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	20	
$I_{DM}^{(1)(3)}$	Drain current (pulsed)	80	A
$I_D^{(4)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	7.4	A
	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	5.2	
I_{DM}	Drain current (pulsed)	29.6	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ °C}$	75	W
P_{TOT}	Total dissipation at $T_{pcb} = 25\text{ °C}$	4.8	
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

Notes:

- (1) This value is rated according to R_{thj-c} .
- (2) Current limited by package.
- (3) Pulse width is limited by safe operating area.
- (4) This value is rated according to $R_{thj-pcb}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.0	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:

- (1) When mounted on a 1-inch² FR-4, 2 Oz copper board, $t < 10\text{ s}$.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, not repetitive	7.4	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	210	mJ

Notes:

- (1) starting $T_j = 25\text{ °C}$, $I_D = I_{AV}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$, $T_{\text{C}} = 125\text{ °C}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 20\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 4\text{ A}$		27	40	m Ω
		$V_{\text{GS}} = 5\text{ V}$, $I_{\text{D}} = 4\text{ A}$		32	50	

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	670	-	pF
C_{OSS}	Output capacitance		-	170	-	
C_{RSS}	Reverse transfer capacitance		-	56	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 25\text{ V}$, $I_{\text{D}} = 7.4\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Gate charge test circuit")	-	22.5	-	nC
Q_{gs}	Gate-source charge		-	2.5	-	
Q_{gd}	Gate-drain charge		-	7	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 30\text{ V}$, $I_{\text{D}} = 3.7\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Switching times test circuit for resistive load" and Figure 19: "Switching time waveform")	-	7	-	ns
t_{r}	Rise time		-	15.4	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	36.8	-	
t_{f}	Fall time		-	7.7	-	

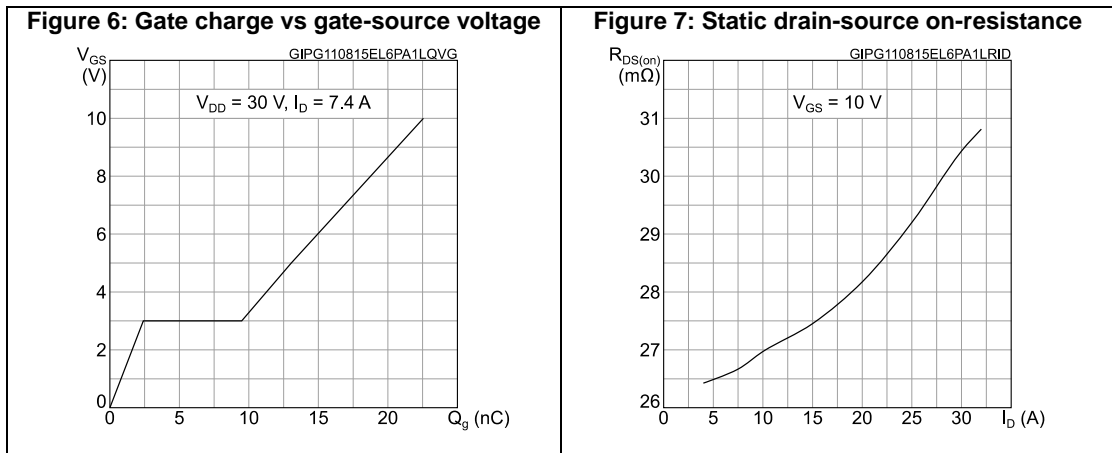
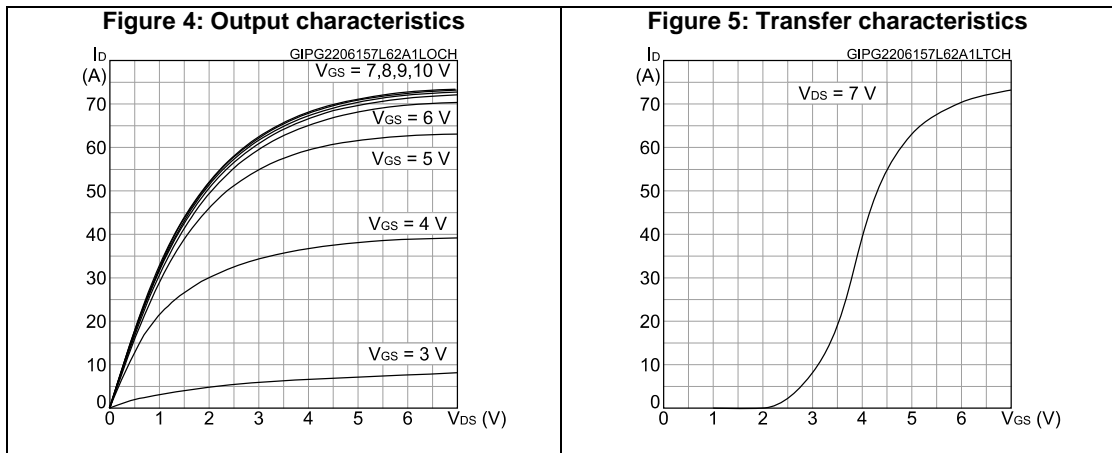
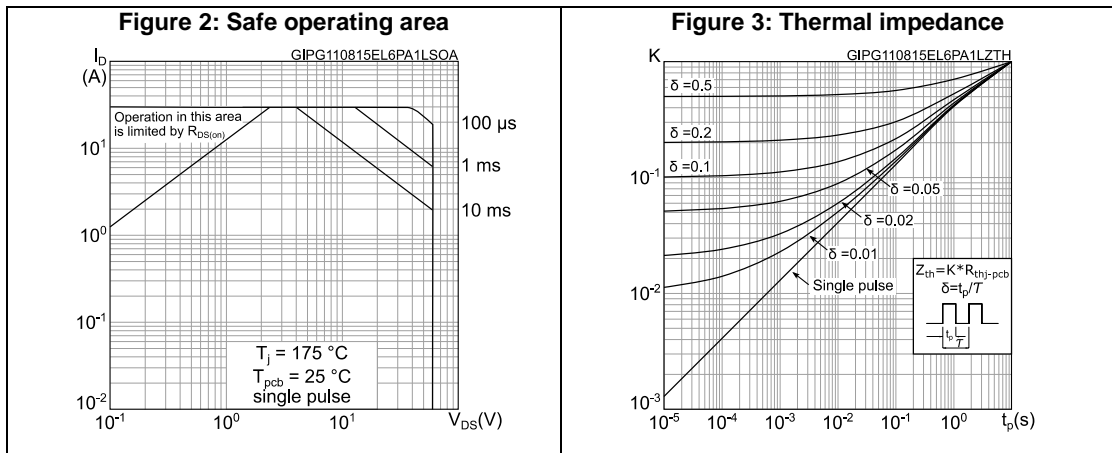
Table 8: Source-drain diode

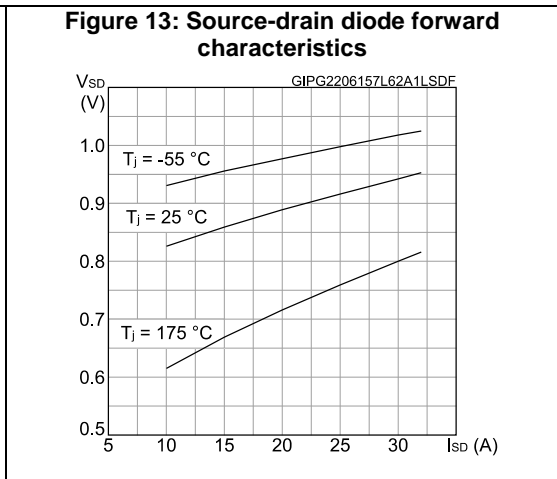
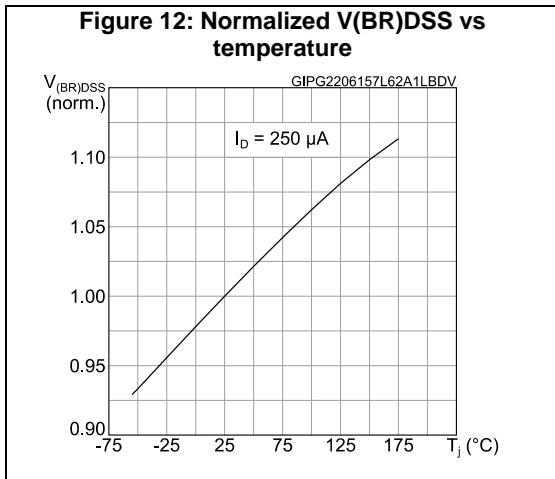
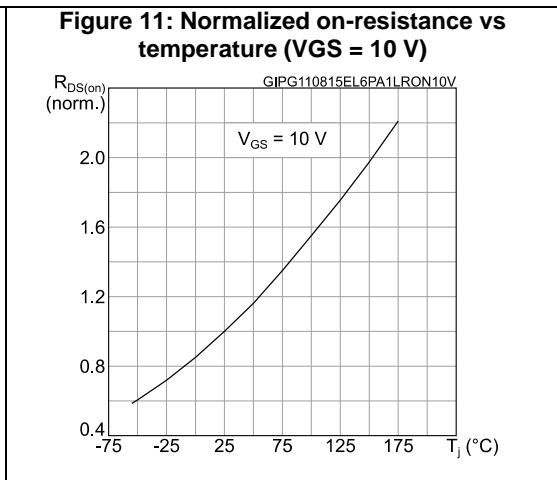
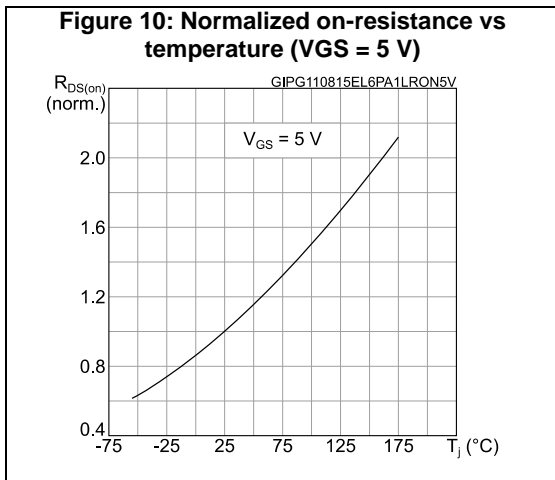
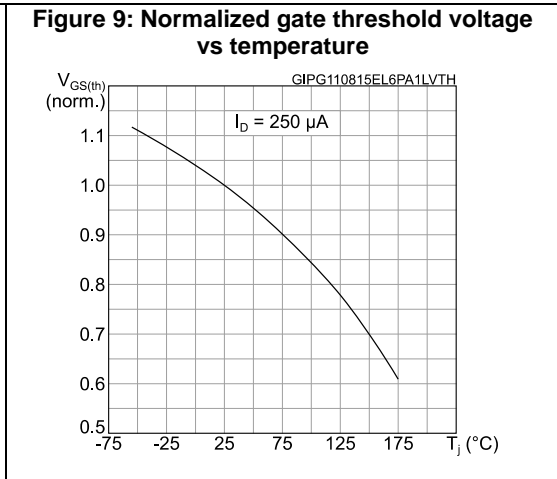
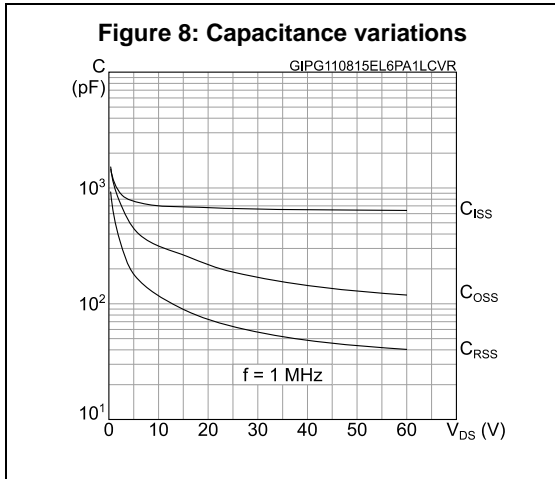
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7.4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		29.6	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 7.4\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 7.4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 48\text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	28		ns
Q_{rr}	Reverse recovery charge		-	31.6		nC
I_{RRM}	Reverse recovery current		-	2.26		A

Notes:

- (1) Pulse width is limited by safe operating area.
(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

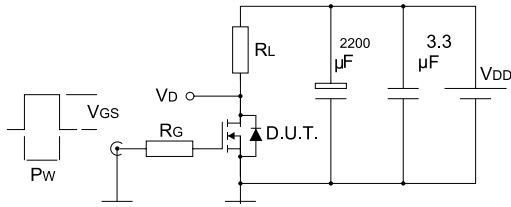
2.1 Electrical characteristics (curves)





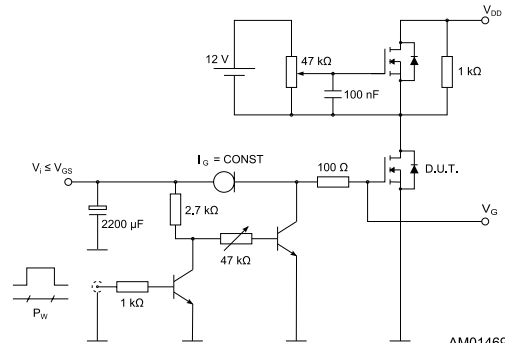
3 Test circuits

Figure 14: Switching times test circuit for resistive load



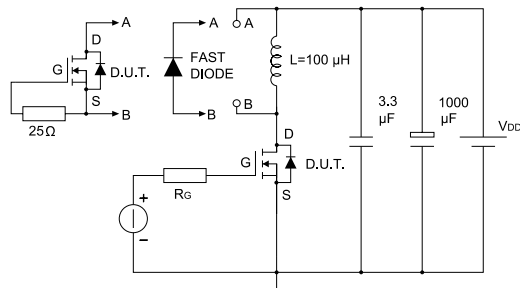
AM01468v1

Figure 15: Gate charge test circuit



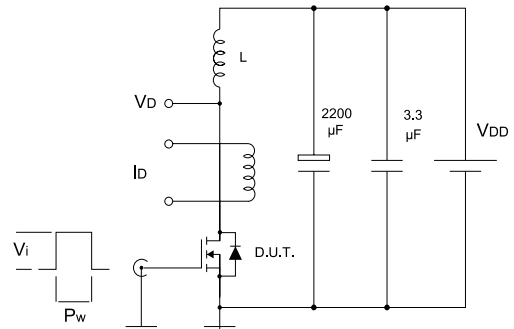
AM01469v1

Figure 16: Test circuit for inductive load switching and diode recovery times



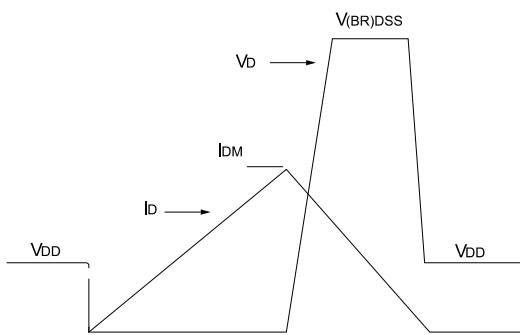
AM01470v1

Figure 17: Unclamped inductive load test circuit



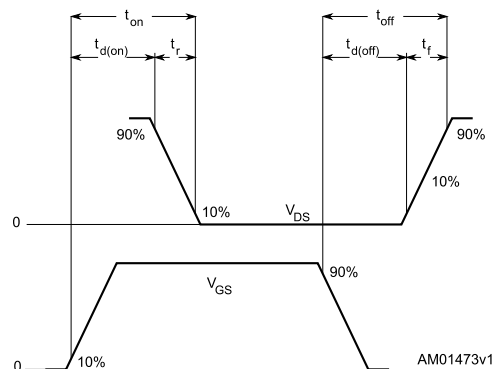
AM01471v1

Figure 18: Unclamped inductive waveform



AM01472v1

Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 20: PowerFLAT™ 5x6 WF type R package outline

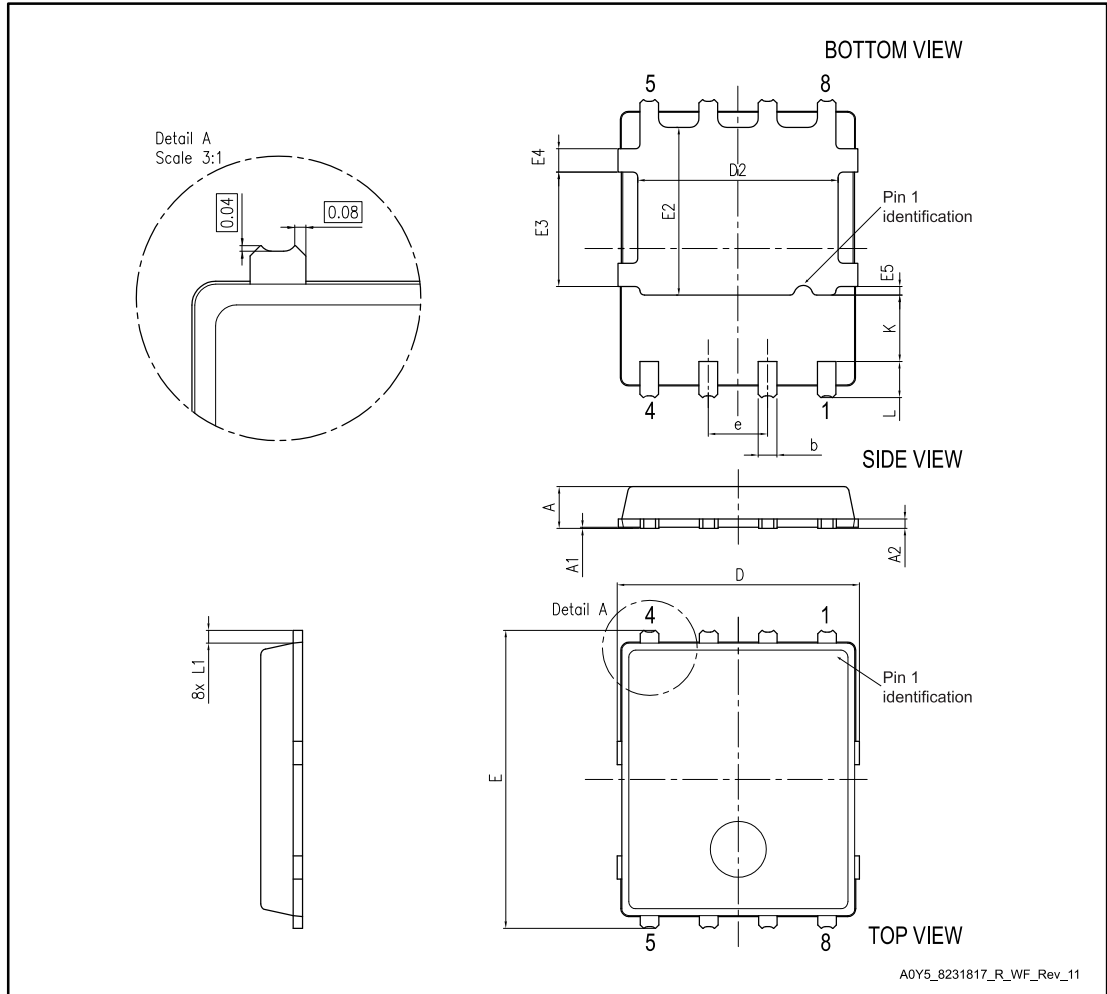
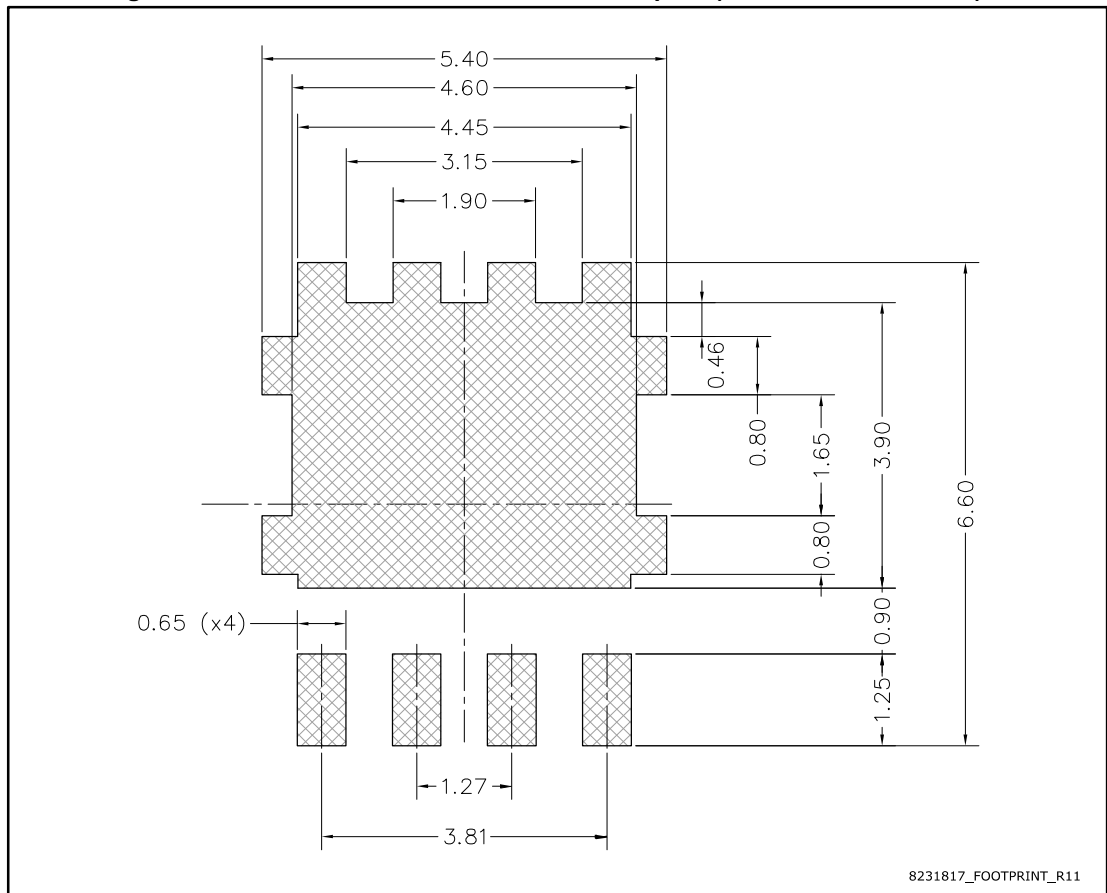


Table 9: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.70		0.90
L1		0.275	
K	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 21: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



8231817_FOOTPRINT_R11

4.2 PowerFLAT™ 5x6 WF packing information

Figure 22: PowerFLAT™ 5x6 WF tape

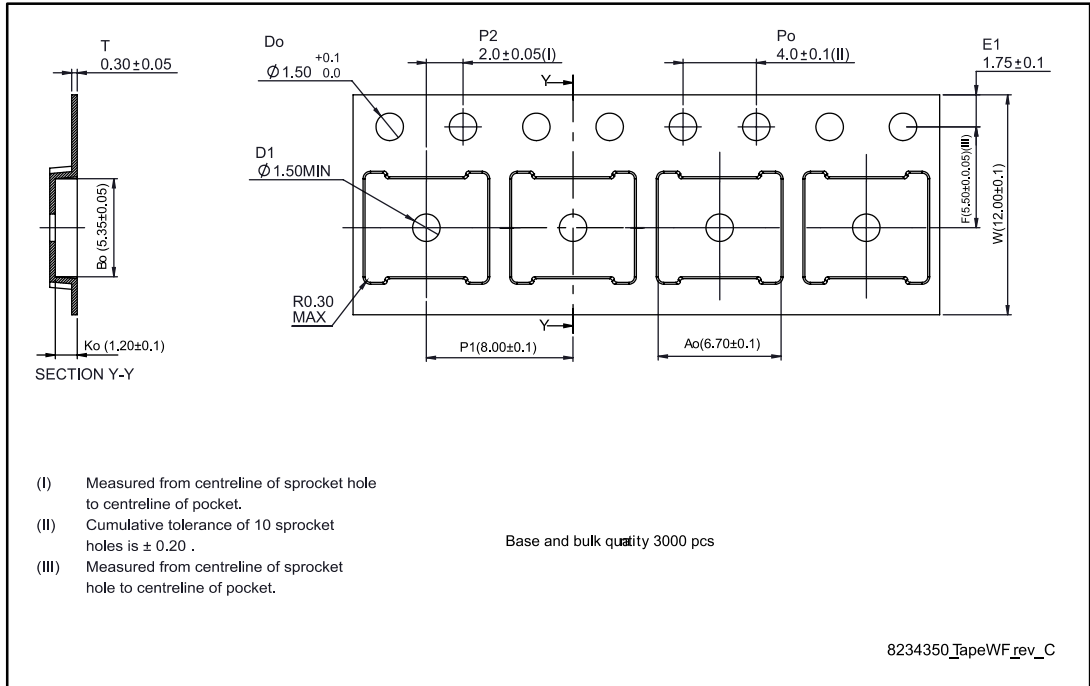


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

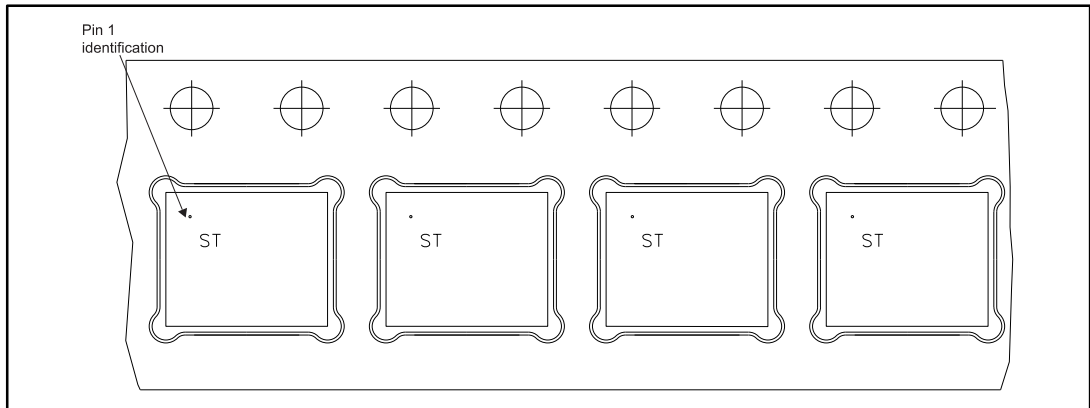
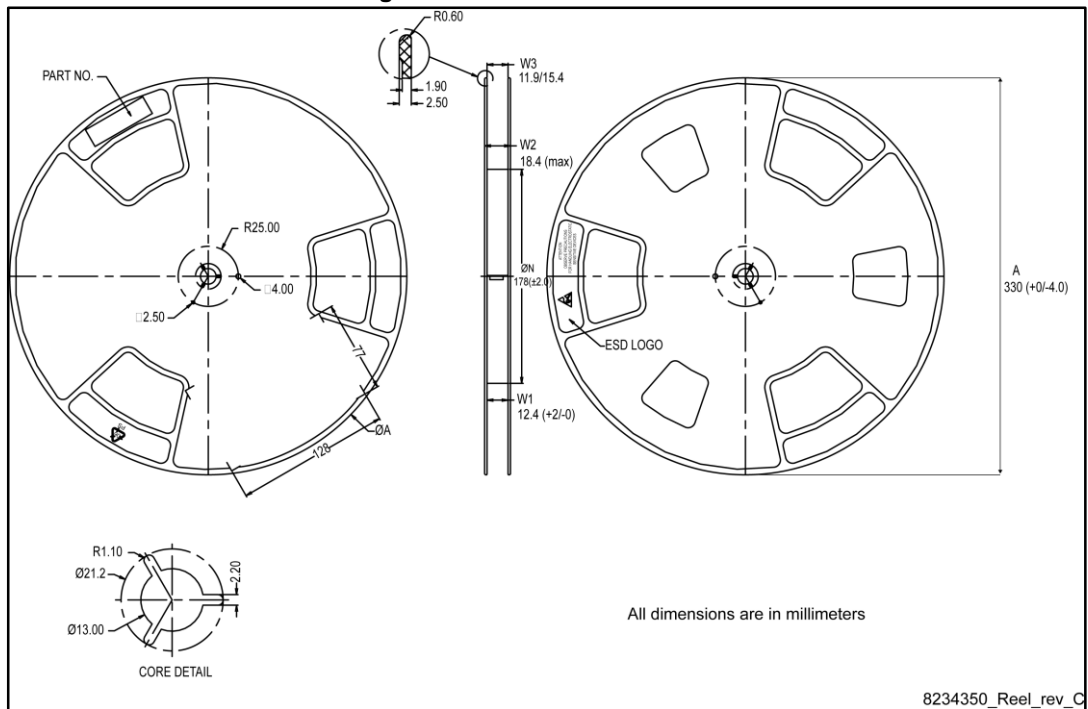


Figure 24: PowerFLAT™ 5x6 reel



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
28-Sep-2015	1	First release.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved